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(54) **VERTICAL BJT FOR HIGH DENSITY MEMORY**

(71) Applicant: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsin-Chu (TW)

(72) Inventors: **Yu-Wei Ting**, Taipei (TW); **Chun-Yang Tsai**, Hsinchu (TW); **Kuo-Ching Huang**, Hsinchu (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsin-Chu (TW)

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Primary Examiner — Min Huang
(74) *Attorney, Agent, or Firm* — Eschweiler & Associates, LLC

(57) **ABSTRACT**

Some aspects of this disclosure relate to a memory device. The memory device includes a collector region having a first conductivity type and which is coupled to a source line of the memory device. A base region is formed over the collector region and has a second conductivity type. A gate structure is coupled to the base region and acts as a shared word line for first and second neighboring memory cells of the memory device. First and second emitter regions are formed over the base region and have the first conductivity type. The first and second emitter regions are arranged on opposite sides of the gate structure. First and second contacts extend upwardly from the first and second emitter regions, respectively, and couple the first and second emitter regions to first and second data storage elements, respectively, of the first and second neighboring memory cells, respectively.

20 Claims, 6 Drawing Sheets